FIG. 1

FIRST PRINCIPLE OF PRESENT INVENTION

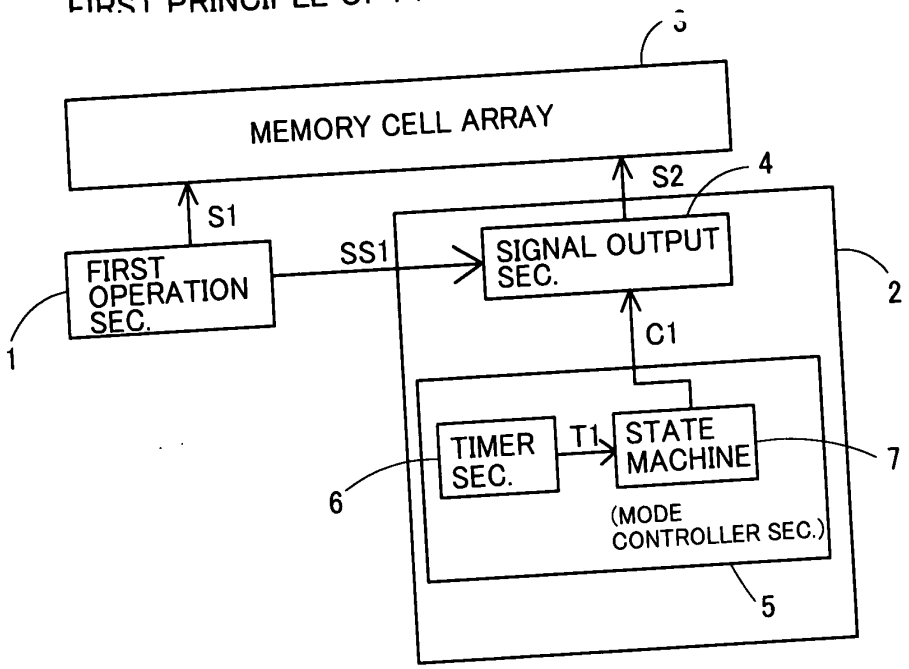

FIG. 2

SECOND PRINCIPLE OF PRESENT INVENTION

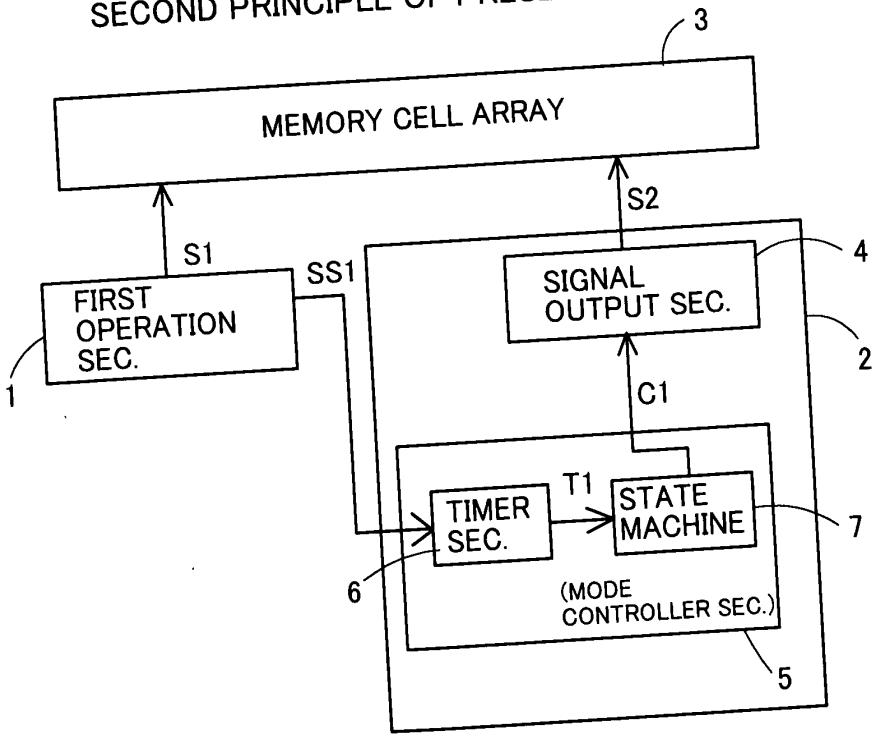

FIG. 3

THIRD PRINCIPLE OF PRESENT INVENTION

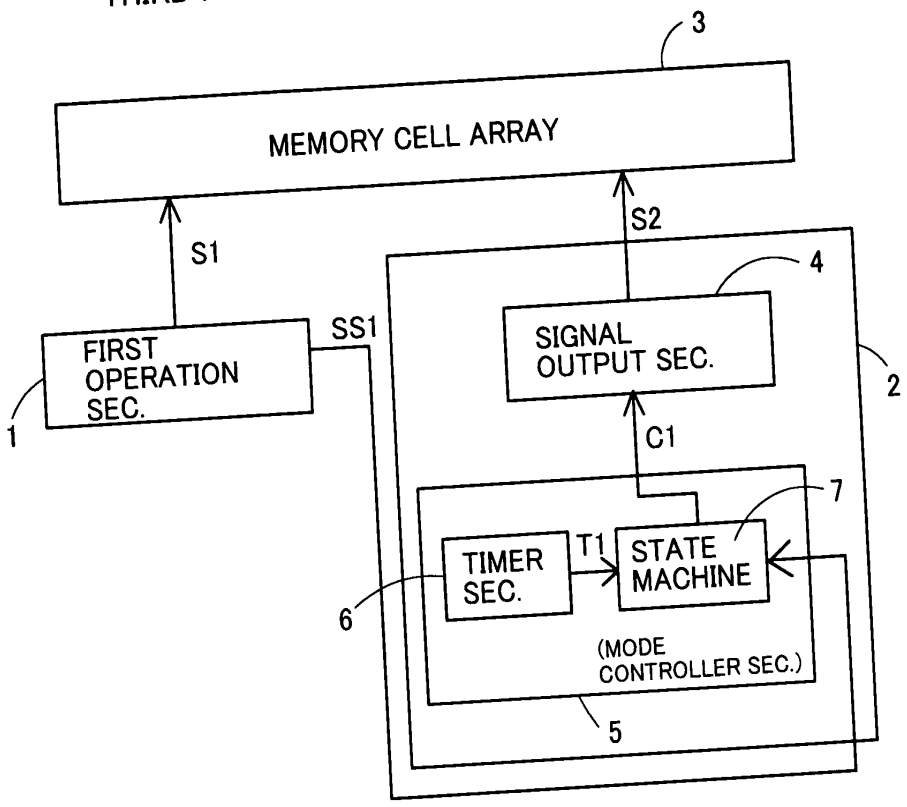

FIG. 4 CIRCUIT BLOCK DIAGRAM OF SEMICONDUCTOR MEMORY DIRECTED TO FIRST EMBODIMENT

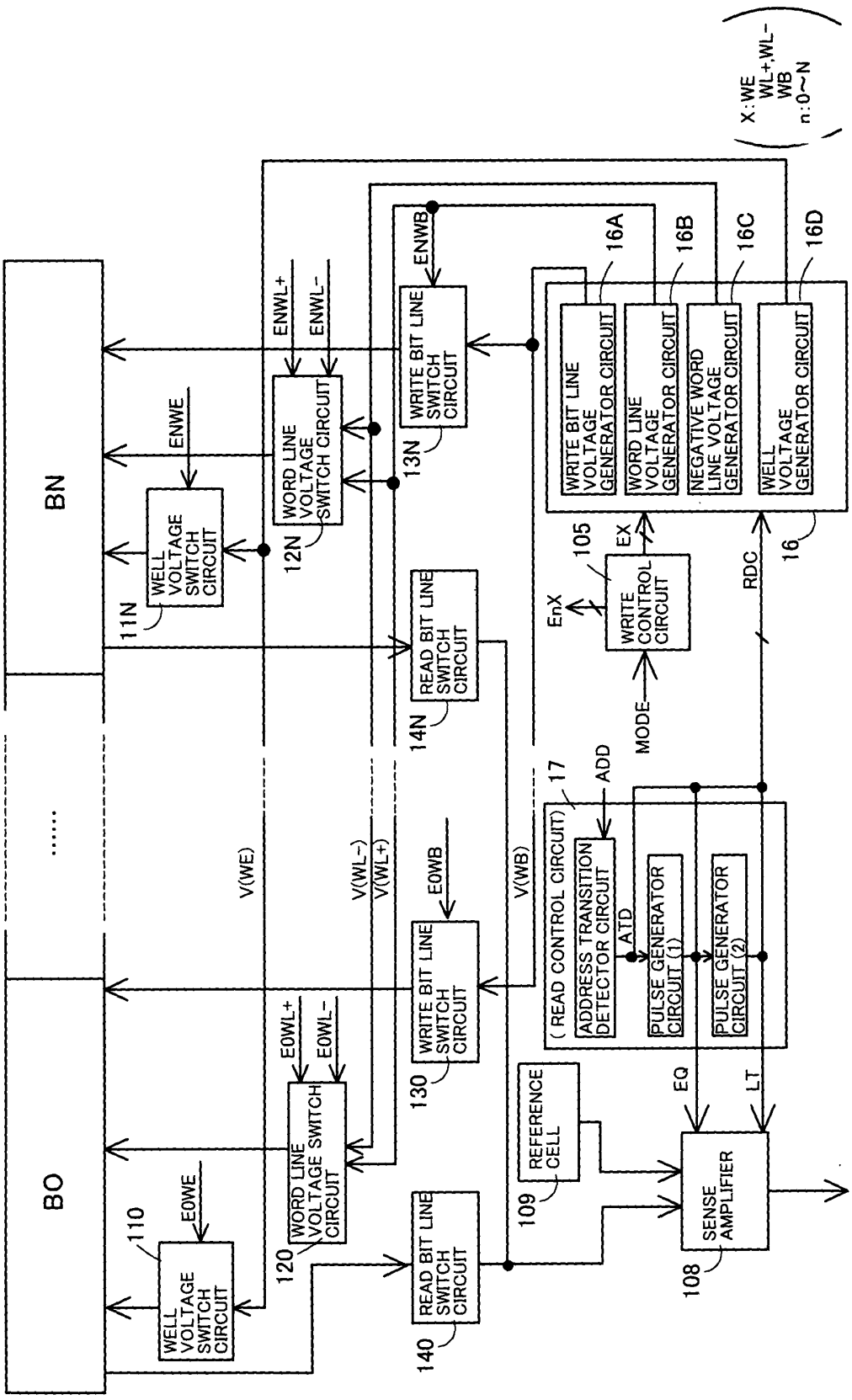

FIG. 5

CIRCUIT DIAGRAM OF FIRST SPECIFIC EXAMPLE DIRECTED TO FIRST EMBODIMENT

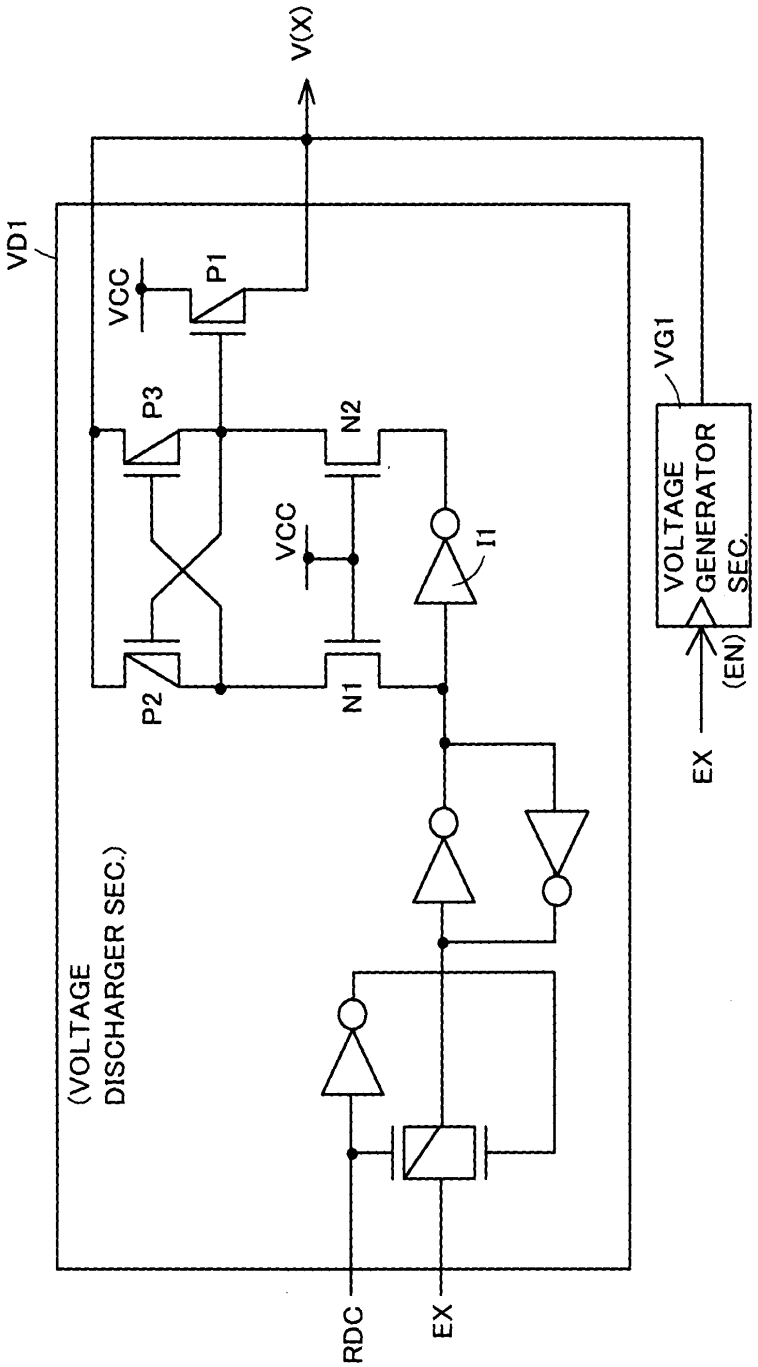

FIG. 6

OPERATIONAL WAVEFORM OF FIRST SPECIFIC EXAMPLE DIRECTED TO FIRST EMBODIMENT

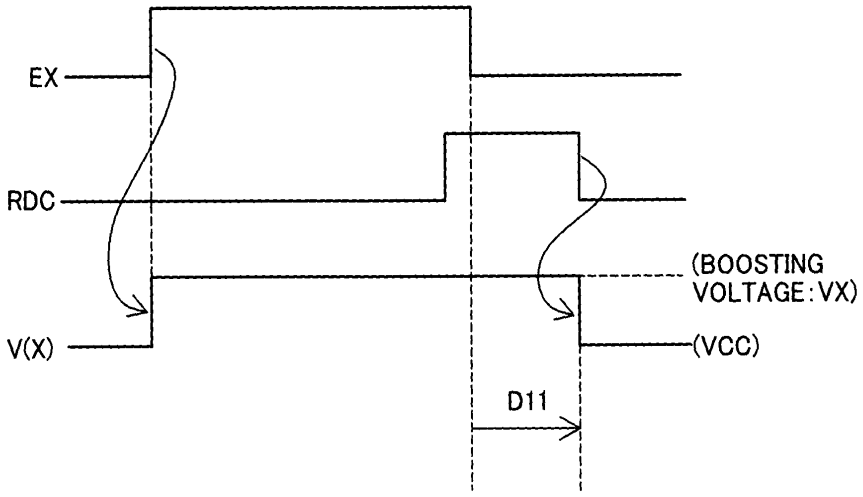

FIG. 7

CIRCUIT DIAGRAM OF SECOND SPECIFIC EXAMPLE DIRECTED TO FIRST EMBODIMENT

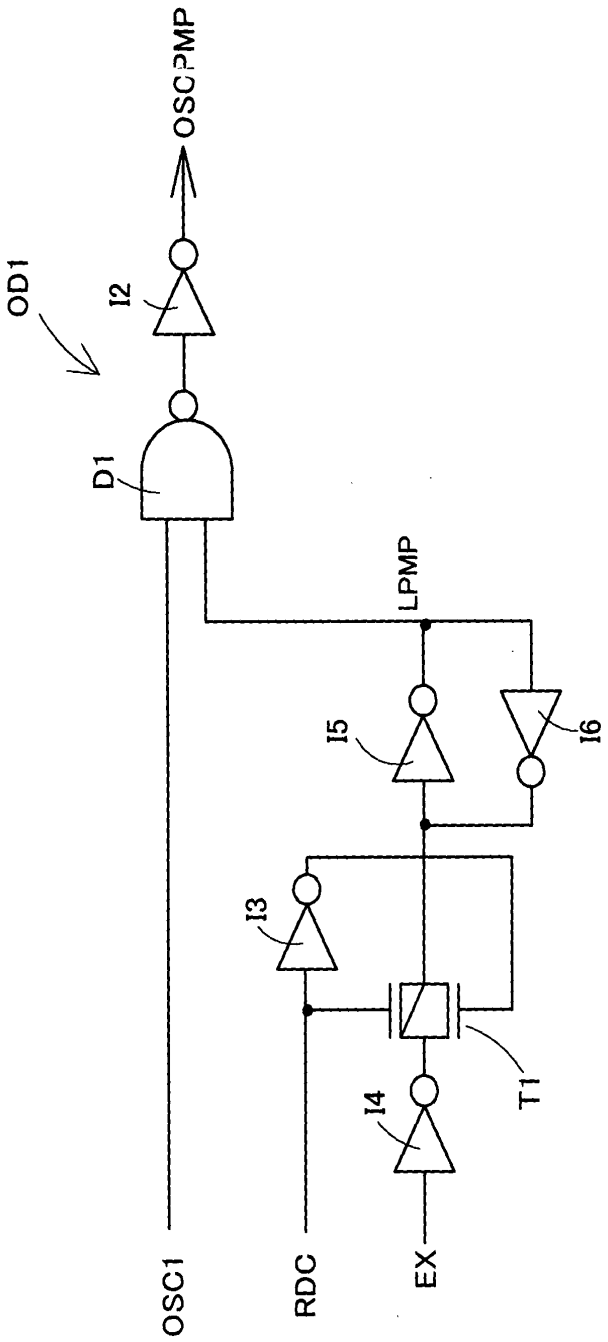

FIG. 8

OPERATIONAL WAVEFORM OF SECOND SPECIFIC
EXAMPLE DIRECTED TO FIRST EMBODIMENT

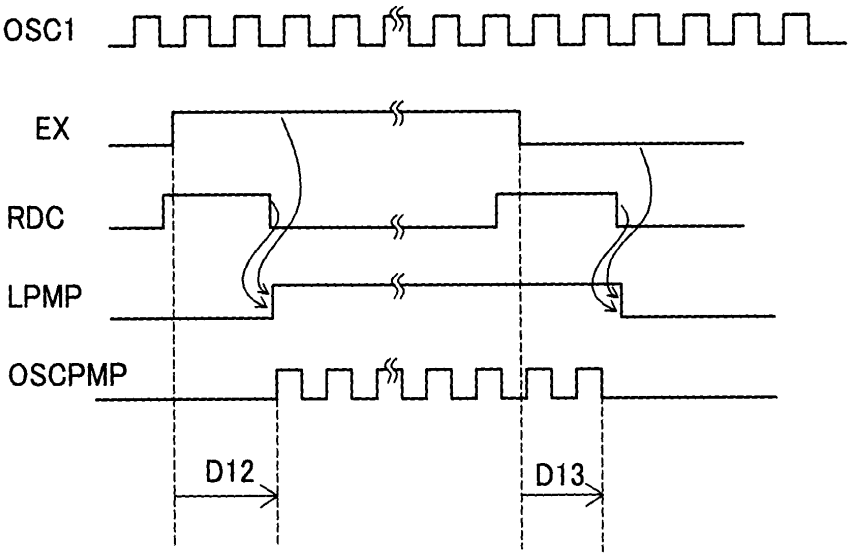

FIG. 9 CIRCUIT BLOCK DIAGRAM OF SEMICONDUCTOR MEMORY DIRECTED TO SECOND EMBODIMENT

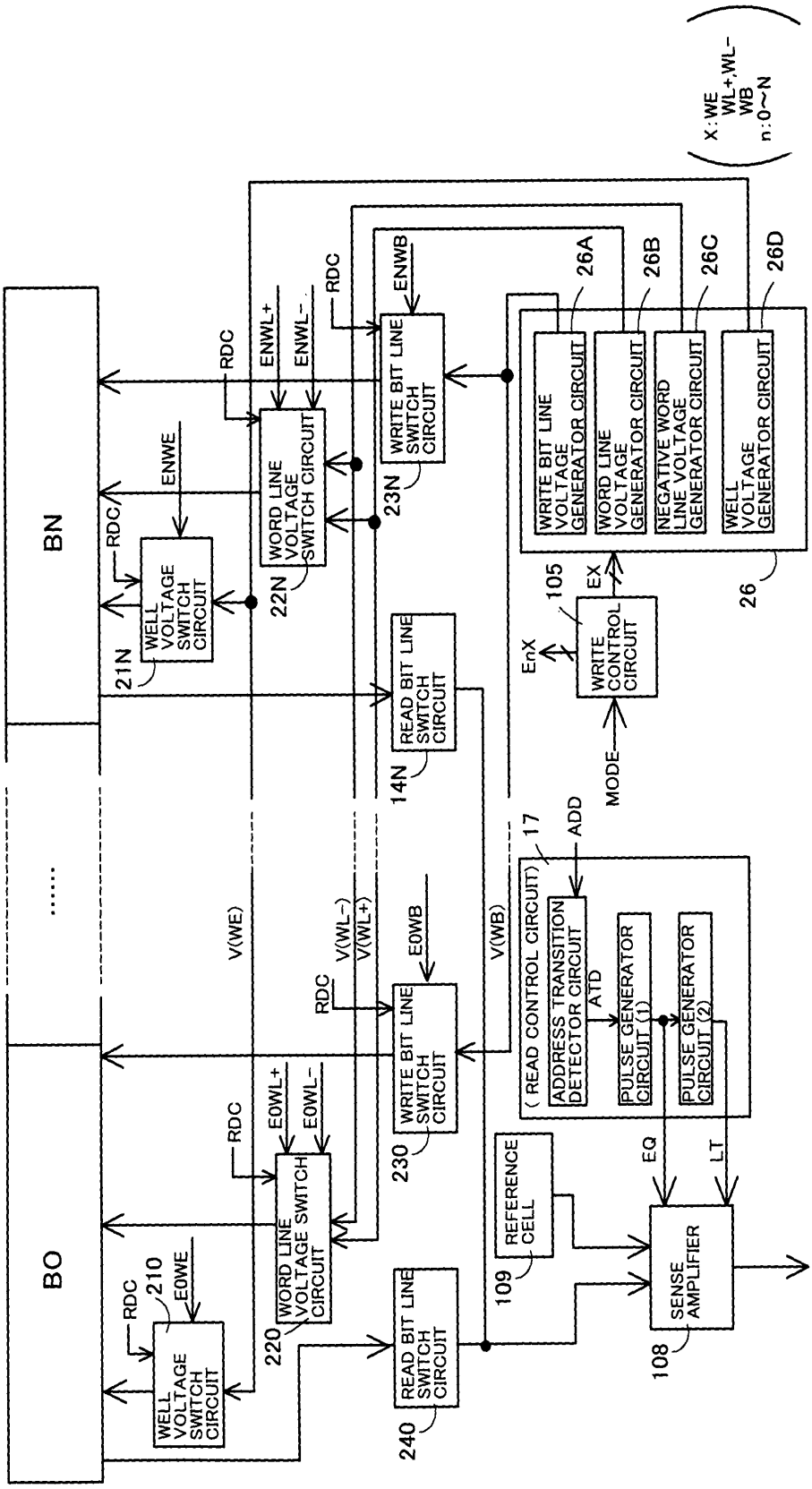

FIG. 10

CIRCUIT DIAGRAM OF SPECIFIC EXAMPLE DIRECTED TO SECOND EMBODIMENT

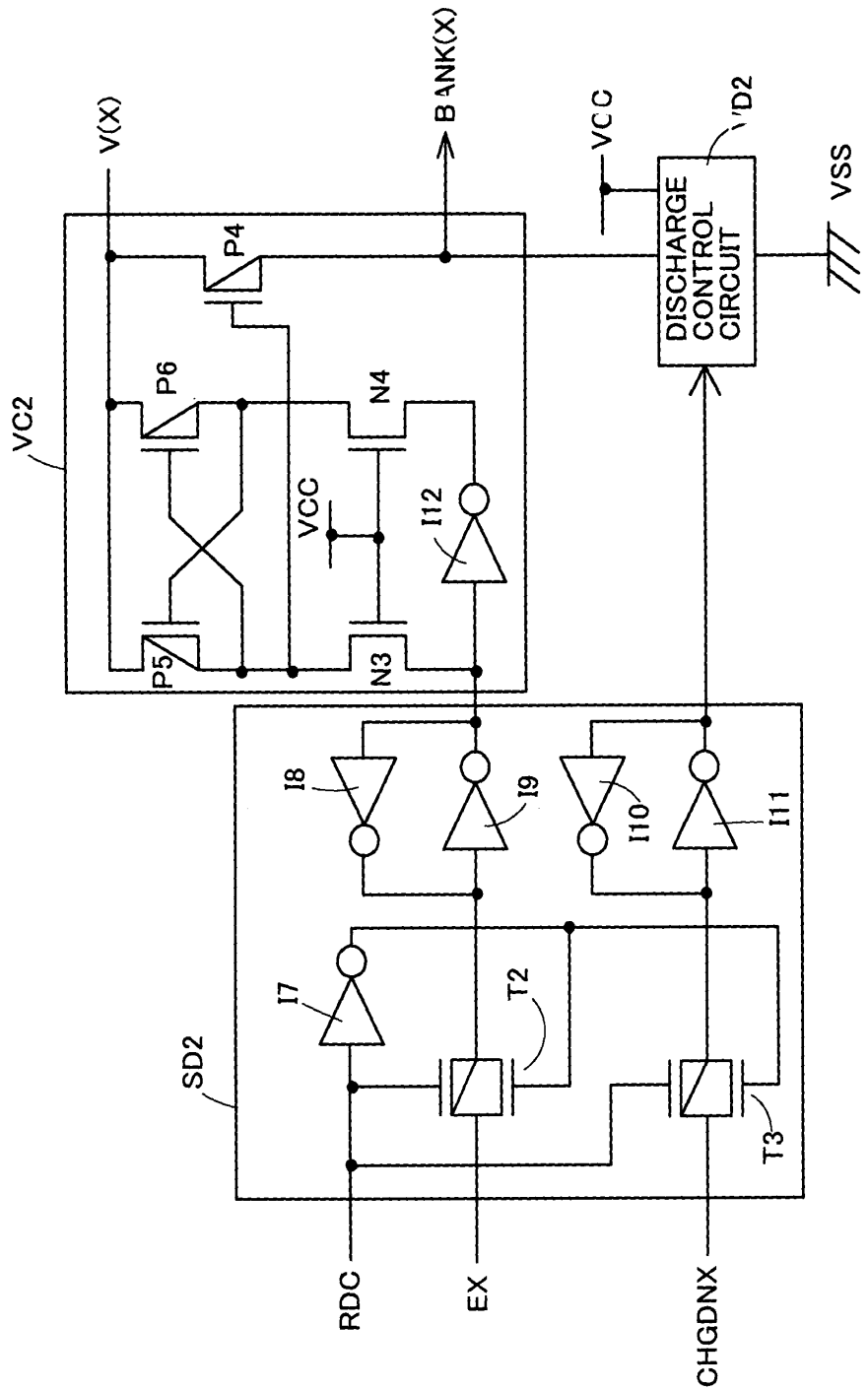

FIG. 11

OPERATIONAL WAVEFORM OF SPECIFIC EXAMPLE DIRECTED TO SECOND EMBODIMENT

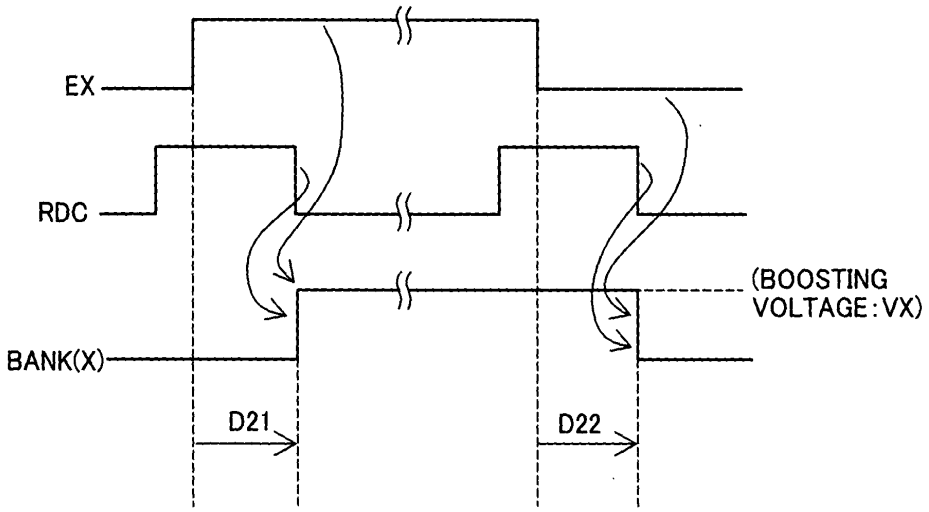

FIG. 12

CIRCUIT BLOCK DIAGRAM OF SEMICONDUCTOR MEMORY DIRECTED TO THIRD EMBODIMENT

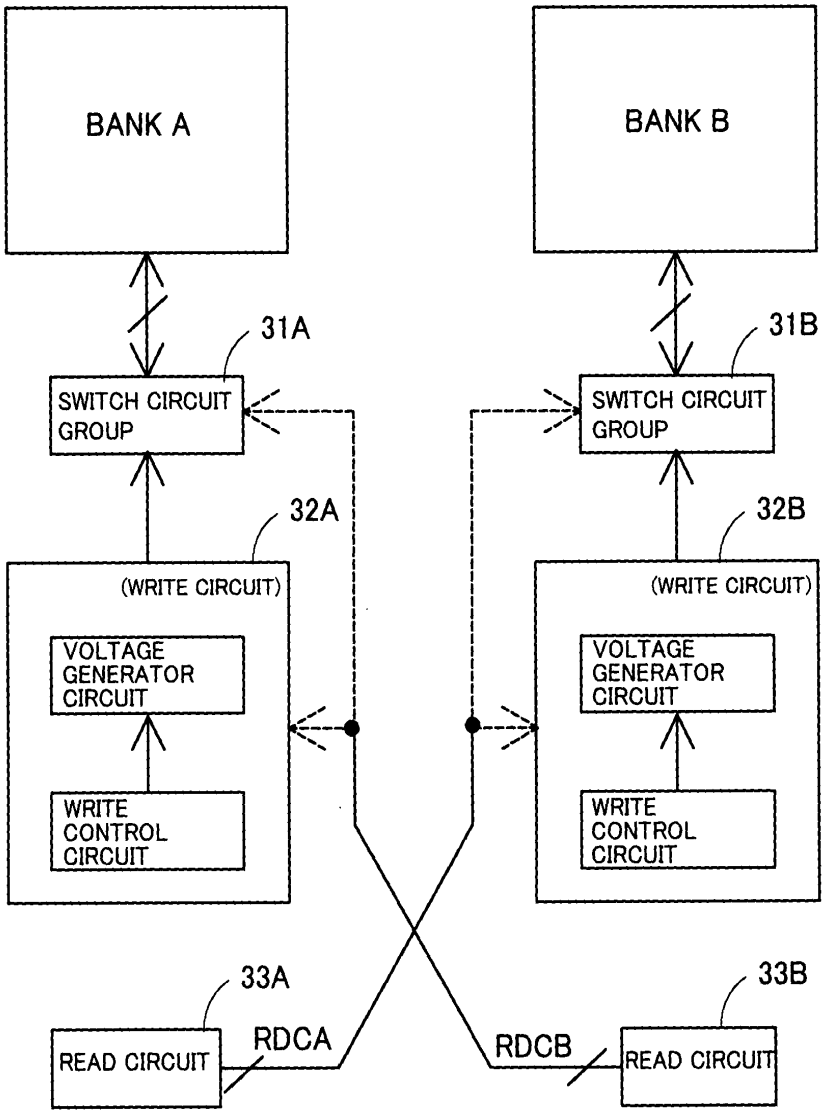

FIG. 13

MODE CONTROL SECTION IN SEMICONDUCTOR MEMORY DIRECTED TO FOURTH EMBOD MENT

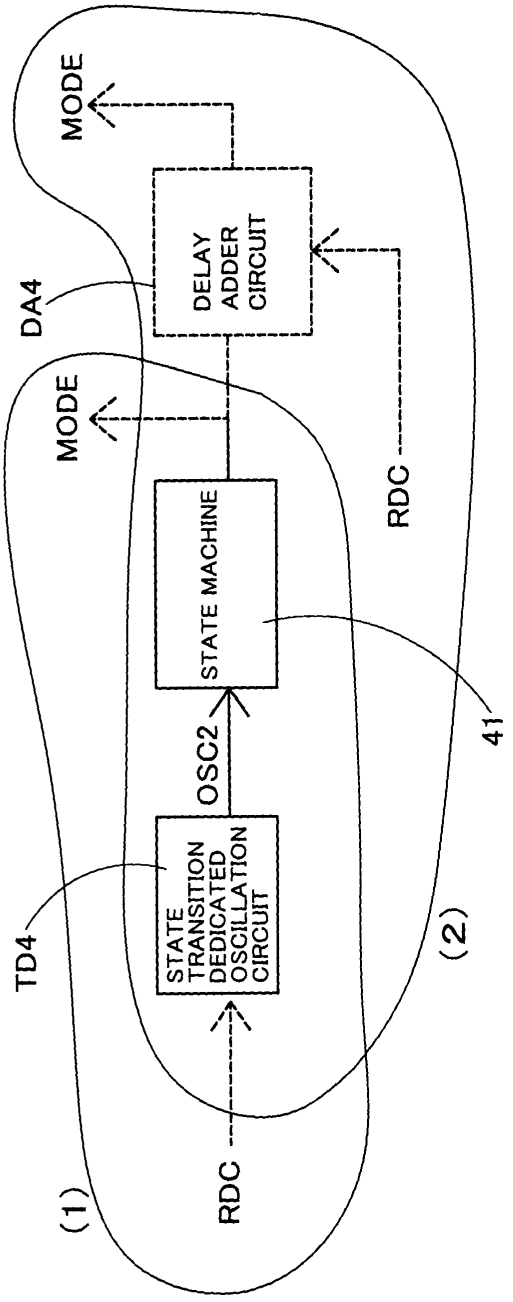

FIG. 14

CIRCUIT DIAGRAM OF FIRST SPECIFIC EXAMPLE DIRECTED TO FOURTH EMBODIMENT

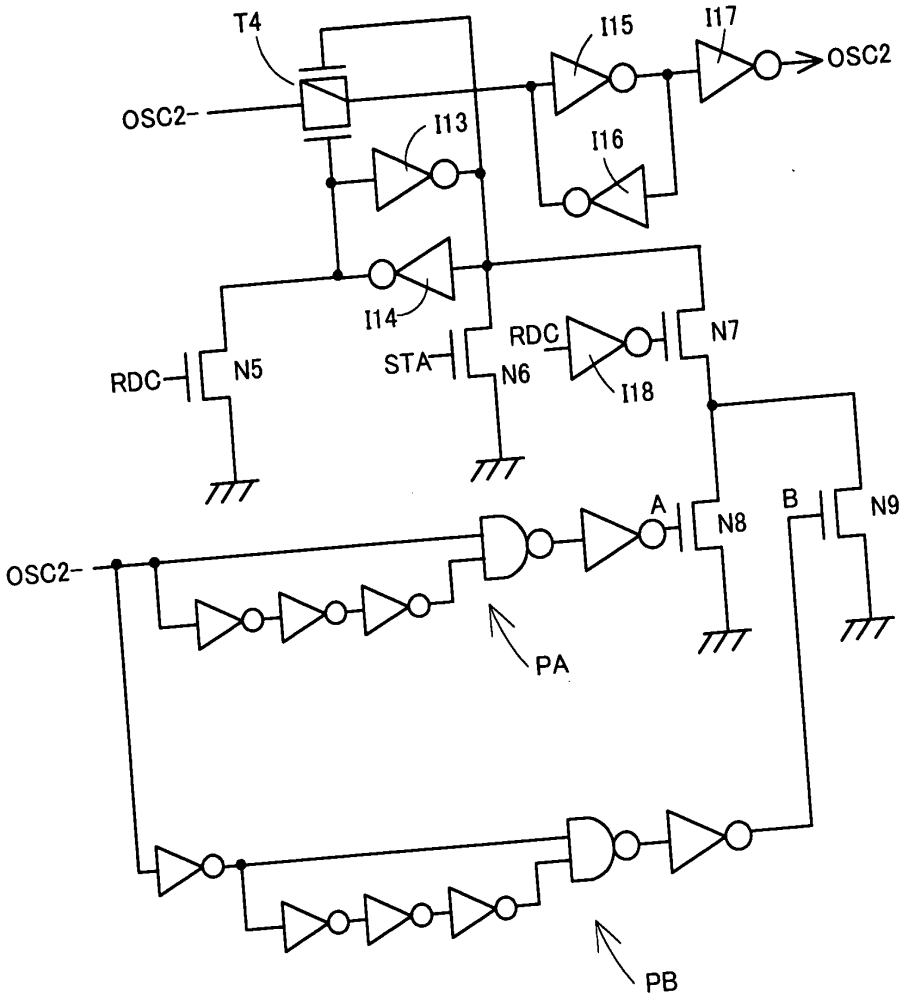

FIG. 15

OPERATIONAL WAVEFORM OF FIRST SPECIFIC EXAMPLE DIRECTED TO FOURTH EMBODIMENT

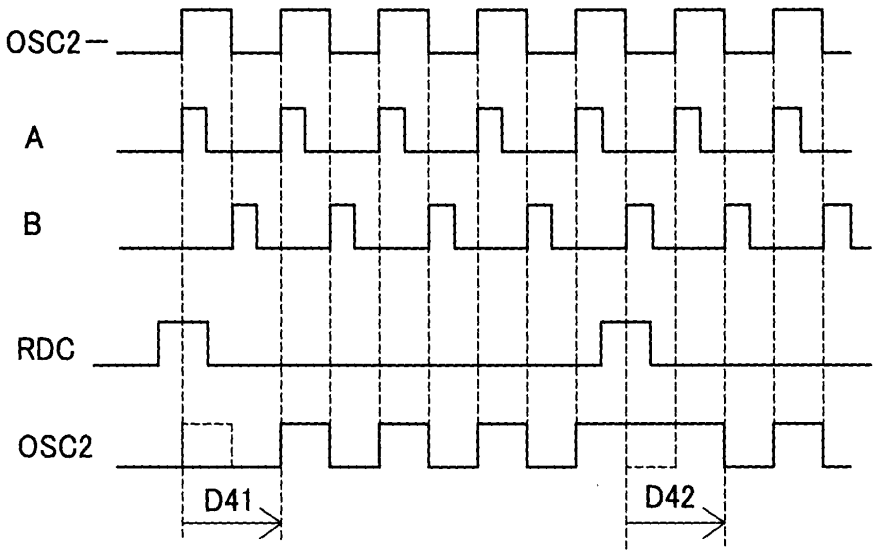

FIG. 16

CIRCUIT BLOCK DIAGRAM OF SECOND SPECIFIC EXAMPLE DIRECTED TO FOURTH EMBODIMENT

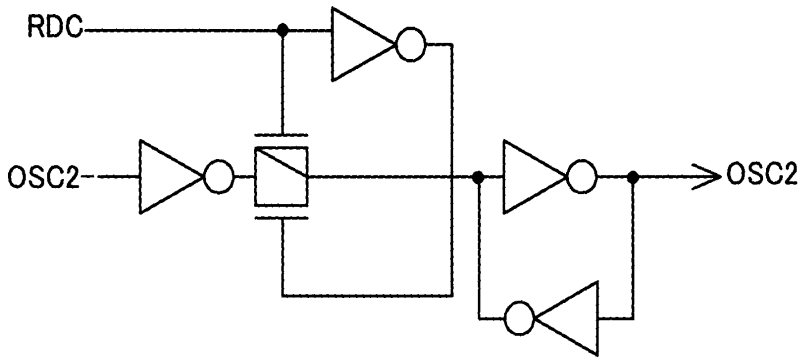

FIG. 17

OPERATIONAL WAVEFORM OF SECOND EXAMPLE DIRECTED TO FOURTH EMBODIMENT

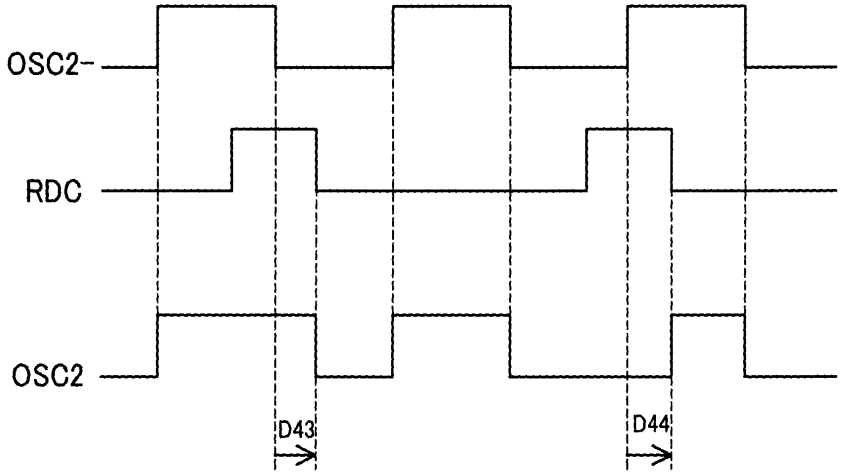

FIG. 18

CIRCUIT DIAGRAM OF THIRD SPECIFIC EXAMPLE DIRECTED TO FOURTH EMBODIMENT

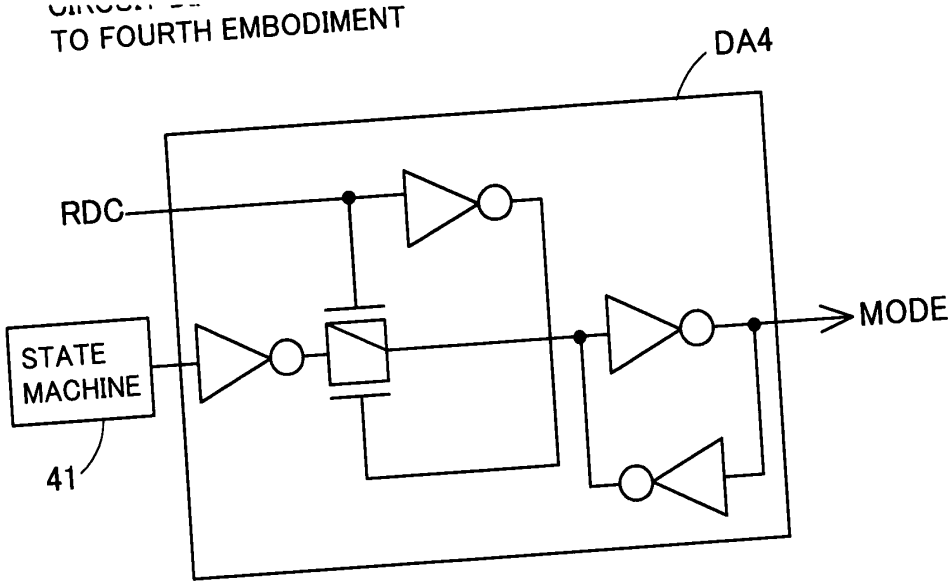

FIG. 19

STATE MACHINE IN SEMICONDUCTOR MEMORY DIRECTED TO FIFTH EMBODIMENT

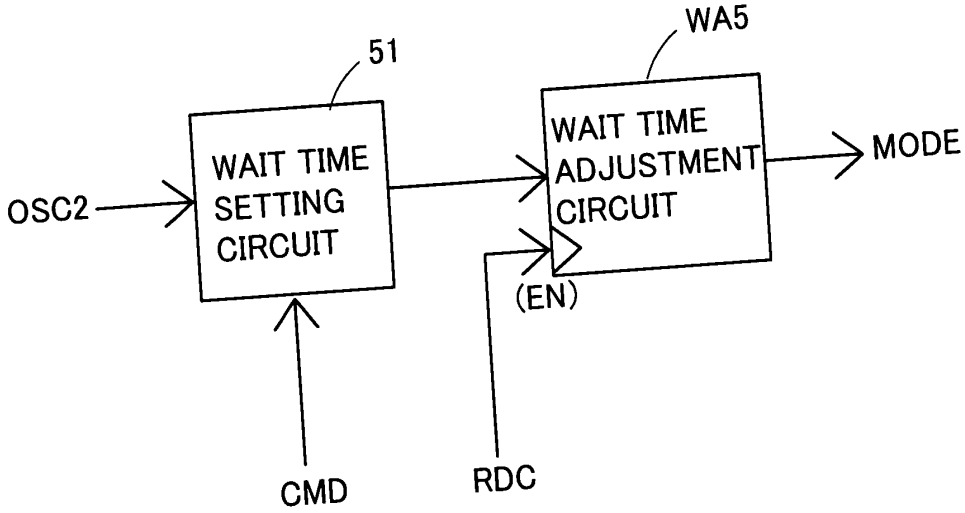

FIG. 20 PRIOR ART

CIRCUIT BLOCK DIAGRAM OF CONVENTIONAL SEMICONDUCTOR MEMORY

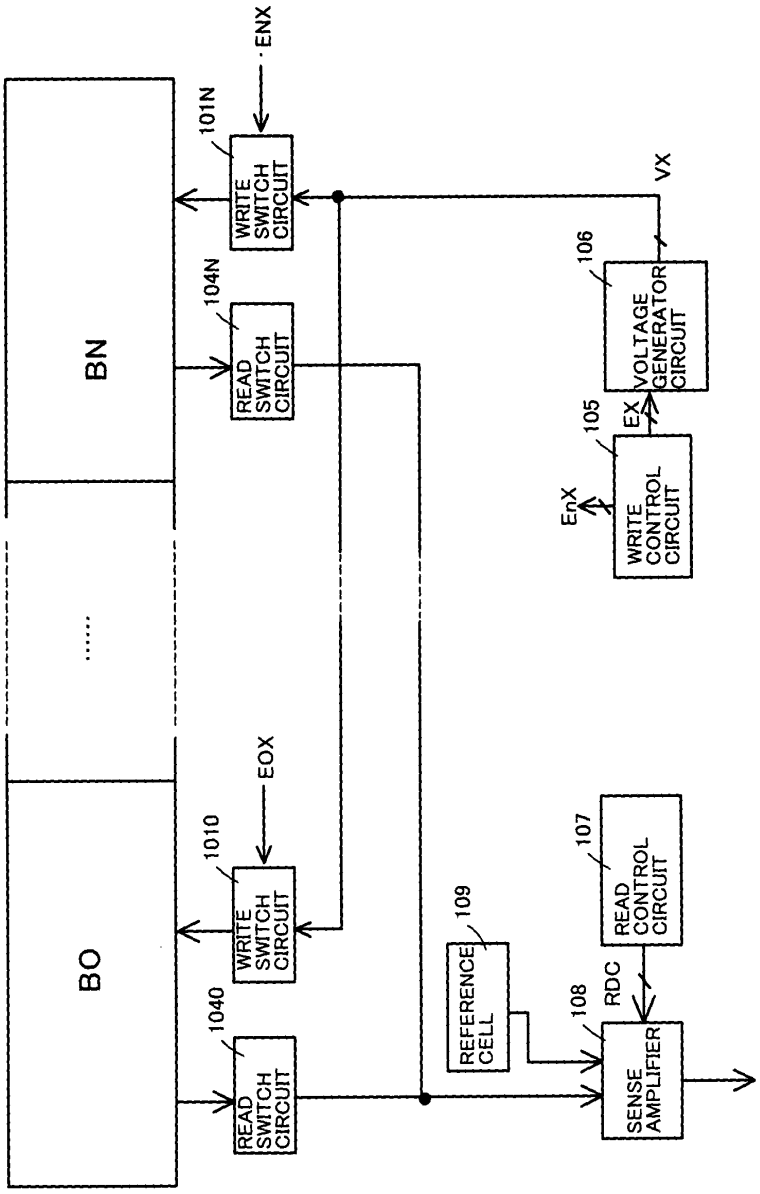

FIG. 21(A)

OPERATIONAL WAVEFORM OF RESPECTIVE FUNCTION MODES

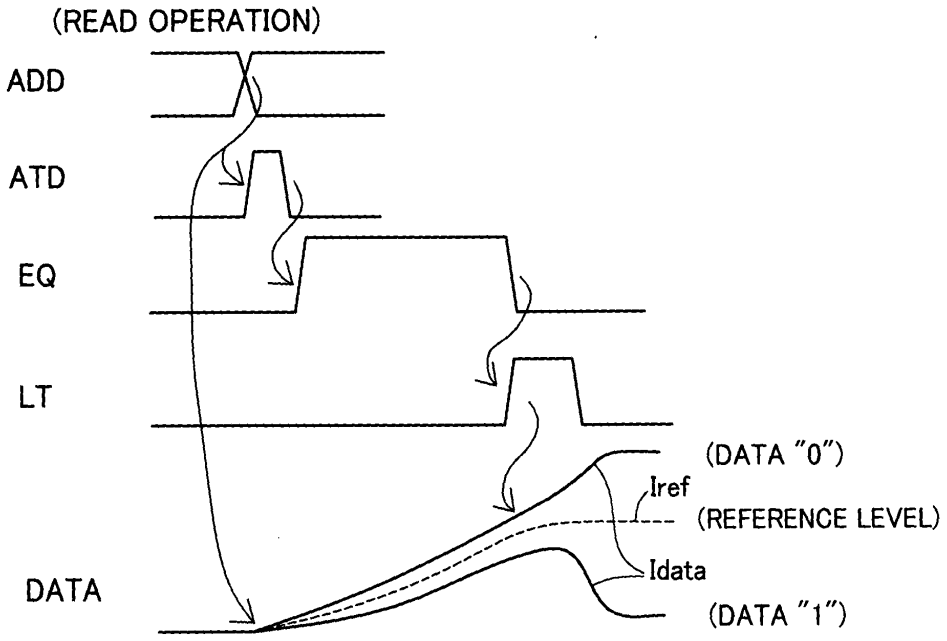

FIG. 21(B)

(PGM OPERATION)

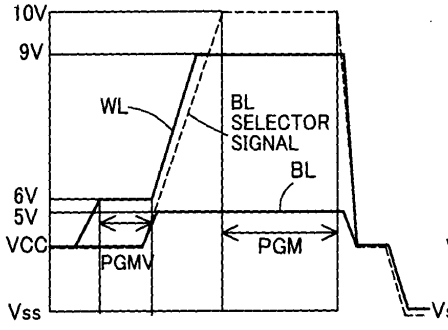

FIG. 21(C)

(ER OPERATION)